## AMENDMENTS TO THE CLAIMS

PENDING CLAIMS:

The following is a complete list of claims with status identifiers:

1-7. (Cancelled)

8. (Currently Amended) A circuit comprising:

a differential sense circuit;

a latch, said latch comprising cross coupled inverters;

said differential sense circuit and said latch being coupled so as to form a differential sense latch such that, in operation, an electronic signal stored in said latch is retained for at least one clock cycle;

further comprising a sense amp, said sense amp and said differential sense latch coupled such that, in operation, differential signals present on differential output terminals of said sense amp cause an electronic signal to be stored in said differential sense latch;

wherein said sense amp comprises an n-type sense amp;

~~The circuit of claim 7,~~ wherein said differential sense circuit comprises:

a first inverter and a second inverter each having stacked n-devices, an input terminal, an output terminal and a clock terminal;

said output ~~terminals~~ terminal of said first inverter and said output terminal of said second inverter being coupled, respectively, to opposite terminals of said latch, said input terminals being coupled, respectively, to a non-inverted output terminal and an inverted output terminal of said n-type sense amp; and

said clock terminals being coupled to a pre-charge clock terminal of said n-type sense amp, wherein said clock terminals of said first and second inverters are further coupled to a respective top n-device of said stacked n-devices in said first and second inverters.

9. The circuit of claim 8, wherein said inverters comprise transistors which, in operation, represent substantially equivalent loads to said inverted and non-inverted output terminals of said n-type sense amp.

10-24. (Cancelled)